

SEMICONDUCTOR PACKAGE BOARD USING A METAL BASE

5 BACKGROUND OF THE INVENTION

(a) Field of the Invention

10 The present invention relates to a semiconductor package board using a metal base, a semiconductor device using the semiconductor package, and a manufacturing method thereof. More specifically, the present invention relates to a semiconductor package board having excellent smoothness in a part on which a semiconductor chip is mounted, thereby improving reliability of the semiconductor device, and to a manufacturing method of such semiconductor package board.

15 (b) Description of the Related Art

Ceramic multilayer wiring boards, each of which mounts thereon a semiconductor chip, for example, enable high-density interconnections to be formed and are widely used. Such ceramic multilayer wiring boards are described in Japanese Patent Laid-open
20 Publication No. Hei. 8-330474. The ceramic multilayer wiring board described in this publication includes an insulating board made of alumina or the like on which a conductor pattern made of a metal having a high melting point such as tungsten or molybdenum is formed. The insulating board is formed with a recess in which a
25 semiconductor chip is received, and the recess is sealed by a covering

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member.

Japanese Patent Laid-open Publication No. Hei. 11-17058 and Japanese Patent No. 2679681 describe a build-up board or a multi-layered printed circuit board, in which organic resin is used for the insulating material, and a fine-pitch circuit is constructed of copper interconnections formed by etching or plating. A multilayer wiring board which uses organic resin for the insulating material is also considered applicable for multi chip modules (MCM) mounted with a large number of semiconductor chips. The build-up board in which thin films of insulating layers are deposited on a printed circuit board in several layers allows a fine-pitch circuit to be formed on a surface layer, and thus offers advantages for increasing the circuit density.

Japanese Patent Laid-open Publication No. 2000-58701 describes a tape-type board in the form of a chip size package (CSP) and a ball grid array (BGA) including a polyimide film on which copper interconnections are formed.

However, the above-mentioned prior art has the following problems. Ceramic used for the insulating board in the ceramic multilayer wiring board is hard and brittle, and consequently it is apt to chip or crack during fabrication and transfer. Chipping or cracking of the board deteriorates the sealing property of the semiconductor chip rendering it defective, and leads to a decrease in the yield of the ceramic multilayer wiring boards.

Generally, the ceramic multilayer wiring board is fabricated by printing electrically conductive patterns on green sheets followed by

stacking them, and then baking the stacked sheets. There is inevitably warpage in the baked board because of the shrinkage caused by baking at a high temperature, resulting in defective products due to deformation or dimensional variations. Such products which do not satisfy the physical requirements cannot provide a high degree of smoothness required for a high-density circuit board or a flip-chip mounting board. That is, physical defects of the board constitute an impediment to a further increase in the number of pins or the density of the circuit and to further miniaturization of the circuit. Poor smoothness in a region where a semiconductor chip is mounted causes cracks or disconnections between the flip-chip mounted semiconductor chip and the board. As a result the reliability of the semiconductor device is lowered.

Build-up boards are apt to warpage because of the mismatches in the coefficient of thermal expansion between the printed circuit board used as a core material and the insulating resin film formed on the board. Such warpage also causes various problems when flip-chip bonding a multi-pinned semiconductor chip impeding further increase in the circuit density. Warpage also decreases the yield of the build-up board.

Tape-type boards made of polyimide have a drawback that position misalignment often occurs because of the expansion of the tape carrier, and therefore it is not suitable for higher density circuit formation.

Moreover, in conventional semiconductor packages, a

semiconductor chip is mounted on a multilayer wiring structure film which is formed on a board. Therefore, the region on which the semiconductor chip is mounted is often undulated because of the multi-layered structure, and consequently the connection between the semiconductor chip and the multilayer wiring structure film is unstable.

Furthermore, conventional semiconductor devices require a stiffener for increasing the rigidity of the board. Where, for example, a large heat sink is provided for covering a plurality of semiconductor chips stiffeners are interposed between the board and the heat sink in the gaps between adjacent semiconductor chips. While the board can have a higher rigidity because of the stiffeners, the provision of such stiffeners makes the fabrication process more complex, and increases the production cost of the semiconductor device.

SUMMARY OF THE INVENTION

In view of the above-described problems in the prior art, it is an object of the present invention to provide an improved semiconductor package board with superior smoothness, and a manufacturing method thereof, for providing a highly reliable semiconductor device which enables further miniaturization of high-pin-contact, high-density circuit, and which requires no stiffener.

A semiconductor package board according to the present invention includes: a metal base plate having an opening suited for receiving therein a semiconductor chip; and a multilayer wiring film

formed on the metal base plate, the multilayer wiring film having a first surface in contact with the metal base plate and mounting thereon a plurality of first metal pads within a region exposed from the opening of the metal base plate.

5 According to the semiconductor package board of the present invention, the multilayer wiring film is laminated on the flat metal base, whereby smoothness of the multilayer wiring film is improved. The metal base also serves to reinforce the multilayer wiring film, so as to restrict deformation thereof and to allow circuits to have a higher
10 density and a smaller width with more pins.

 A semiconductor device according to the present invention includes the above-described semiconductor package board, and a semiconductor chip received in the opening in the metal base and electrically connected to the first metal pads of the semiconductor
15 package board.

 According to the semiconductor device of the present invention, the semiconductor chip is received in the opening formed in the metal base and connected on the top surface of the multilayer wiring film, whereby the reliability of the connection between the semiconductor
20 chip and the multilayer wiring film is improved.

 A method for manufacturing a semiconductor package board according to the present invention includes the steps of: forming a plurality of first metal pads on a first surface of a metal base plate; forming a multilayer wiring film including a plurality of insulating
25 layers and a plurality of wiring layers on the first surface of the metal

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base plate, the multilayer wiring film having a plurality of second metal pads on a top surface thereof, each of the plurality of second metal pads being electrically connected to the respective first metal pads through the wiring layers; and forming an opening in the metal
5 base plate suited for receiving therein a semiconductor chip, the opening exposing the first metal pads.

According to the method of the present invention, the multilayer wiring film is laminated on a planar metal base which serves as a support, after which the opening is formed in the metal
10 base in a region in which the semiconductor chip is to be received. This improves smoothness of the multilayer wiring film, particularly the smoothness of the surface thereof on which the semiconductor chip is mounted.

A method for manufacturing a semiconductor device according
15 to the present invention includes the step of connecting a semiconductor chip to the first metal pads of the semiconductor package board fabricated through the above-described process.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Figs. 1A to 1C illustrate a semiconductor device according to a first embodiment of the present invention, Fig. 1A being a perspective view showing the front surface thereof, Fig. 1B being a perspective view showing the rear surface thereof, and Fig. 1C being a partial sectional view thereof;

25 Fig. 2 is a partial sectional view showing a semiconductor

device according to a second embodiment of the present invention;

Fig. 3 is a partial sectional view showing a semiconductor device according to a third embodiment of the present invention;

Fig. 4 is a partial sectional view showing a semiconductor device according to a fourth embodiment of the present invention;

Fig. 5 is a partial sectional view showing a semiconductor device according to a fourth embodiment of the present invention.

Figs. 6A to 6C illustrate a semiconductor device according to a fifth embodiment of the present invention, Fig. 5A being a perspective view showing the front surface thereof, Fig. 5B being a perspective view showing the rear surface thereof, and Fig. 5C being a partial sectional view thereof;

Fig. 7 is a partial sectional view showing a semiconductor device according to a sixth embodiment of the present invention;

Fig. 8 is a partial sectional view showing a semiconductor device according to a seventh embodiment of the present invention;

Figs. 9A to 9I are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a first example of the method of the present invention;

Figs. 10A to 10K are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a second example of the method of the present invention;

Figs. 11A to 11E are partial sectional views showing steps of a process for fabricating a semiconductor device according to a modification of the second example of the method of the present

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invention;

Figs. 12A to 12J are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a third example of the method of the present invention;

5 Figs. 13A to 13J are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a fourth example of the method of the present invention;

10 Figs. 14A to 14J are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a fifth example of the method of the present invention;

Figs. 15A and 15B are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a sixth example of the method of the present invention;

15 Figs. 16A to 16G are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a seventh example of the method of the present invention;

20 Figs. 17A to 17C are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to an eighth example of the method of the present invention;

Figs. 18A to 18E are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a ninth example of the method of the present invention;

25 Figs. 19A to 19C are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device

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according to a tenth example of the method of the present invention;

Figs. 20A to 20G are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to an eleventh example of the method of the present

5 invention; and

Figs. 21A to 21H are partial sectional views consecutively showing steps of a process for fabricating a semiconductor device according to a twelfth example of the method of the present invention.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, the present invention is more specifically described with reference to accompanying drawings, wherein similar constituent elements are designated by similar reference numerals. First, several
15 embodiments of the semiconductor package and the semiconductor device according to the present invention will be described.

Referring to Figs. 1A to 1C, a semiconductor device according to a first embodiment of the present invention includes a full-grid ball grid array (BGA) chip 16 mounted on a multilayer wiring film 15
20 within a central opening of a metal base 11.

The metal base 11 having the central opening and the multilayer wiring film 15 mounted on the metal base 11 in combination constitute a semiconductor package board 31a of the present embodiment. The metal base 11 is formed as a metal plate attached
25 with the multilayer wiring film 15. The opening of the metal base 11

receives therein the semiconductor chip 16, which is mounted on the multilayer wiring film 15. On the rear surface (top surface) of the multilayer wiring film 15 opposite from the front surface thereof where the metal base 11 and the semiconductor chip 16 are arranged, there are provided an array of second metal pads 29, on which an array of solder balls 19 which form a BGA structure are mounted.

On the front surface of the multilayer wiring film 15 on which the metal base 11 and the semiconductor chip 16 are arranged within the central opening of the metal base 11, there are formed a plurality of first metal pads 12 for mounting thereon the semiconductor chip 16. The first metal pads 12 are connected to solder balls 18 formed on the bottom surface of the semiconductor chip 16. The multilayer wiring film 15 includes a plurality of wiring layers 14 each having a predetermined interconnect pattern and insulating resin filling the space of the pattern, and a plurality of insulating layers 13 arranged alternately with the wiring layers 14 and made of organic resin.

The multilayer wiring film 15 is formed on the metal base 11 by using build-up techniques such as subtractive, semi-additive, or full-additive methods. The subtractive method involves etching a copper foil formed on a board or resin for forming a circuit pattern, as, for instance, described in Japanese Patent Laid-open Publication No. Hei. 10-51105. The semi-additive method involves forming a power supply layer or conductive layer, precipitating a metallic layer by electrolytic plating using the conductive layer within a resist pattern, and etching the conductive layer after removing the resist pattern to

form a circuit pattern. The semi-additive method is described in Japanese Patent Laid-open Publication No. Hei. 9-64493, for example. The full-additive method involves forming a resist pattern after catalyst seeding the surface of a board or resin, and forming a circuit pattern by electroless plating using the resist as an insulating layer. The full-additive method is described in Japanese Patent Laid-open Publication No. Hei. 6-334334, for example.

The semiconductor chip 16 is fitted into the recess formed by the opening in the metal base 11 on the front surface of the multilayer wiring film 15. Its solder balls 18 are connected to the first metal pads 12 of the multilayer wiring film 15. The gaps between the solder balls 18 in the space between the semiconductor chip 16 and the multilayer wiring film 15 are filled with under-filling layer 17.

The BGA solder balls 19 are connected to the second metal pads 29, which are connected to the uppermost layer of the wiring layers 14. The wiring layers 14 are each connected through the via holes formed in the insulating layers 13, and the lowest layer of the wiring layers 14 is also connected to the first metal pads 12 through the via holes. The first metal pads 12 are connected to the semiconductor chip 16 through the solder balls 18.

The metal base 11 may be composed of at least one metal which is selected from the group consisting of stainless steel, iron, nickel, copper, and aluminum, or an alloy thereof. Stainless steel and copper alloy are the most preferable in terms of feasibility of handling. The metal base 11 has a preferred thickness in the range of 0.1 to 1.5

mm.

The surface of the first metal pads 12 on which the solder balls 18 are connected for mounting the semiconductor chip 16 may be preferably implemented by a metal such as gold, tin, solder, or an alloy thereof. In the preferred embodiment, the surfaces of the metal pads 12 are composed of gold. In the example illustrated in Fig. 1C, the contact surfaces between the metal pads 12 and the solder balls 18 are coplanar with the surface of the multilayer wiring film 15.

Alternatively, the surface of the metal pads 12 may be recessed from the surface of the multilayer wiring film 15 to securely hold the solder balls 18 therein by allowing the formed recess to function as a dam for the solder ball 18.

The insulating layers 13 are made of either one or more types of organic resin selected from the group consisting of an epoxy resin, an epoxy acrylate resin, an urethane acrylate resin, a polyester resin, a phenol resin, a polyimide resin, a benzocyclobutene (BCB), and a polybenzoxazole (PBO). One of the organic resins may be used for all of the insulating layers 13 interposed between the wiring layers 14.

Alternatively, insulating layers 13 using two or more of the organic resins may be mixed, and interposed between the wiring layers 14.

For example, as in the preferred embodiment, polyimide resin alone may be used for all of the insulating layers 13, or while the lowest insulating layer 13 is made of polyimide resin, the other layers may be formed of epoxy resin.

The wiring layers 14 are preferably made of copper due to its

low cost as in this preferred embodiment. However, other types of metal selected from the group consisting of gold, silver, aluminum, and nickel, or an alloy thereof, are also appropriate.

The semiconductor device according to the first embodiment of the present invention, as described above, includes the semiconductor package board 31a and the semiconductor chip 16 mounted thereon, and is assembled as follows. The semiconductor chip 16 is flip-chip bonded for connecting its solder balls 18 to the respective metal pads 12. The space between the semiconductor chip 16 and the multilayer wiring film 15 is filled by underfill 17, which is cured after the introduction thereof. The BGA solder balls 19 are then mounted onto the metal pads 29 of the multilayer wiring film 15 and thus the semiconductor device shown in Fig. 1A is obtained. The drawing shows an example in which the semiconductor chip 16 is flip-chip bonded via the solder balls 18 connected to the metal pads 12. However, semiconductor chip 16 may be mounted on the surface of the multilayer wiring film 15 with its face upward, and electrically connected to the multilayer wiring film 15 by any suitable means such as wire bonding or the like.

Since the above described semiconductor package board has its multilayer wiring film 15 layered upon the metal base 11, the smoothness of the multilayer wiring film 15 which is achieved is excellent. The semiconductor chip 16 is received within the opening formed in the metal base 11 and connected on the uppermost surface of the planar, warp-free multilayer wiring film 15. In this way a

stable and highly reliable connection between the semiconductor chip 16 and the multilayer wiring film 15 is achieved.

Moreover, the top surface of the semiconductor chip 16 on the side on which it is not connected to the multilayer wiring film 15 is coplanar with the surface of the metal base 11 on the front surface on which it is not bonded to the multilayer wiring film 15. Thereby, the metal base 11 also functions as a stiffener for restricting displacement of the multilayer wiring film 15 in a vertical direction and for enhancing its resistance to buckling. The top surface of the semiconductor chip 16 and the front surface of the metal base 11 are not necessarily coplanar with each other, in which case the metal base 11 can also be used as a frame for preventing deformation of the multilayer wiring film 15. Furthermore, the metal base 11 can function as a topmost ground layer due to its conductivity.

Next, a semiconductor package board or a semiconductor device according to a second embodiment of the present invention will be described. Fig. 2 is a partial sectional view showing the structure of the semiconductor device using the semiconductor package board according to the present embodiment. The characteristic feature of the semiconductor package board according to the present embodiment is that a metallic film 35 is formed on the multilayer wiring film 15 at the periphery of the central opening of the metal base 11.

In the semiconductor device of the present embodiment, the semiconductor chip 16 is mounted on the semiconductor package

board 31b within the central opening of the metal base 11. This structure is formed as follows. Specifically, the semiconductor chip 16 is disposed within the central opening of the metal base 11, and subjected to flip-chip bonding to the metal pads 12 disposed within the central opening by using solder balls 18. Subsequently, the underfill (or underfilling layer) 17 is formed in the space between the semiconductor chip 16 and the multilayer wiring film 15 by filling fluid underfill and subsequent solidification thereof. Thereafter, the BGA solder balls 19 are mounted on the metal pads 29 of the multilayer wiring film 15, thereby achieving the structure of the semiconductor device of Fig. 2. Alternatively, the connection between the semiconductor chip 16 and the multilayer wiring film 15 may be implemented by a wire bonding technique, as in the case of the first embodiment.

In the structure of the second embodiment, the metal film 35 formed on the multilayer wiring film 15 at the periphery of the opening of the metal base 11 alleviates the stress applied to the multilayer wiring film 15, the stress being generated due to the presence of the metal base on which the multilayer wiring film 15 is formed. This suppresses generation of cracks in the multilayer wiring film 15.

Next, a semiconductor package board according to a third embodiment of the present invention will be described. Fig. 3 is a partial sectional view showing the structure of the semiconductor device using the semiconductor package board according to the

present embodiment. The characteristic feature of the semiconductor package board according to the present embodiment is that solder balls 20 are provided on the surface of the metal pads 12 so as to protrude from the surface of the multilayer interconnection film 15.

5 The semiconductor device according to the third embodiment of the present invention includes a semiconductor package board 31c and a semiconductor chip 16 mounted thereon, and is assembled as follows. The semiconductor chip 16 is flip-chip bonded through solder balls 20 to the metal pads 12 arranged within the opening in the
10 metal base 11. The semiconductor chip 16 may have the solder balls 18, in which case it is connected to the metal pads 12 through both the solder balls 18 and 20. The space between the semiconductor chip 16 and the multilayer wiring film 15 is filled by underfilling liquid 17, and the underfilling liquid 17 is cured. The BGA solder balls 19
15 are then mounted onto the metal pads 29 of the multilayer wiring film 15 and thus the semiconductor device shown in Fig. 2 is obtained. Similarly to the first embodiment, the semiconductor chip 16 may be mounted on the multilayer wiring film 15 by wire bonding or the like.

According to the semiconductor device of the present
20 embodiment, solder balls 20 are provided which can function as the main or supplemental solder to flip-chip bond the semiconductor chip 16 to the multilayer wiring film 15, thereby enabling the flip chip pads to be formed at a fine-pitch. Also, the solder balls 18 of the semiconductor chip 16 can be dispensed with. Apart from the solder
25 balls 20, the structure of the semiconductor device according to the

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present embodiment is similarly to that of the above-described first or second embodiment.

Next, a semiconductor package board or a semiconductor device according to a fourth embodiment of the present invention will be described. Fig. 4 and Fig. 5 are partial sectional views showing the structure of the semiconductor device using the semiconductor package board according to the present embodiment. The characteristic feature of the semiconductor package board according to the present embodiment is that thin-film capacitors 21 are mounted on the metal pads 12.

The thin-film capacitors 21 are formed by any suitable techniques such as sputtering, evaporation, CVD, or the anodic oxidation method. They are preferably composed of a compound material having a perovskite structure such as titanium oxide, tantalum oxide, Al_2O_3 , SiO_2 , Nb_2O_5 , BST ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$), PZT ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$), PLZT ($\text{Pb}_{1-y}\text{La}_y\text{Zr}_x\text{Ti}_{1-x}\text{O}_3$), and $\text{SrBi}_2\text{Ta}_2\text{O}_9$, where $0 \leq x \leq 1$, $0 < y < 1$. Alternatively, the thin-film capacitors 21 may be composed of organic resin or the like with which a desired dielectric constant can be achieved.

Due to such thin-film capacitors 21 provided on the metal pads 12, decoupling capacitors can be placed in close proximity to the semiconductor chip 16 in the semiconductor device according to the fourth embodiment. Similarly to the third embodiment, the semiconductor device may also have solder balls 20 on the surface of the metal pads 12 as shown in Fig. 5. Similarly to the first through

third embodiments, the semiconductor chip 16 may be mounted on the multilayer wiring film 15 by wire bonding or the like. Apart from the thin-film capacitors 21, the structure of the semiconductor device according to the present embodiment is similar to that of the above-described first through third embodiments.

Next, a semiconductor package board (or a semiconductor device) according to a fifth embodiment of the present invention will be described. Figs. 6A to 6C illustrate a semiconductor package board or a semiconductor device according to the present embodiment of the present invention. Fig. 6A is a perspective view showing the semiconductor device viewed from the front surface. Fig. 6B is a perspective view illustrating the rear surface of the semiconductor device, and Fig. 6C is a partial sectional view of the semiconductor device. The semiconductor device shown in Figs. 6A through 6C employs a printed circuit board 24 as a carrier base.

The characteristic feature of the semiconductor package board 31c of the fifth embodiment shown in Figs. 6A through 6C is that the semiconductor package boards 31a, 31b or 31b according to the first through third embodiments are provided with the printed circuit board 24 employed as a carrier base. Electrical connection between the package boards 31a or 31b and the printed circuit board 24 is achieved by an anisotropic conductive film or conductive paste 23. For such a carrier base, a printed circuit board composed of more than one layer, a ceramic board, or an organic/inorganic composite board such as, for example, GVP (Grid Via Plate) made by NGK Insulators, LTD, may

be used.

The carrier base may be bonded to the semiconductor package board by any suitable means such as an adhesive, thermo-compressive bonding, or chemical reaction. The electrical connection is achieved by the anisotropic conductive film or conductive paste 23 in a desired pattern. In the example illustrated in Figs. 6A through 6C, a printed circuit board 24 is used for the carrier base, and the printed circuit board 24 is electrically connected to the multilayer wiring film 15 via the conductive paste 23 and the metal pads 29 through the through-holes 30 in the printed circuit board 24. Electrical connection between the printed circuit board 24 and the multilayer wiring film 15 is not necessarily be effected via the through-holes 30, and instead, the printed circuit board 24 may have connection pads on its surface for such purpose. Alternatively, the through-holes 30 in the printed circuit board 24 may be filled with insulating resin, and metal pads may be formed on the surface of this insulating resin for the electrical connection. Further, the through-holes 30 may be filled with a paste containing metal particles. The conductive paste 23 shown in Fig. 6C may be sealed by covering the conductive paste 23 with insulating resin.

The semiconductor device according to the fifth embodiment is composed of the semiconductor package board 31c and a semiconductor chip 16 mounted thereon, and is assembled as follows. The printed circuit board 24 is bonded by an adhesive 22 to a semiconductor package board 31a, 31b or 31c of the above described

first through fourth embodiments. In this way the electrical connection is achieved in the desired positions, thereby obtaining the semiconductor package board 31c as shown in Figs. 6A to 6C. The semiconductor chip 16 is flip-chip bonded so as to be electrically
5 connected to the metal pads 12 of the semiconductor package board 31c. Electrical connection of the semiconductor chip 16 with the semiconductor package board 31c may be achieved through the above mentioned solder balls 20 if such are formed on the metal pads 12, or alternatively through the solder balls 18 in the absence of the solder
10 balls 20. Or alternatively, both of the solder balls 18 and 20 may be used for connecting the semiconductor chip 16 to the metal pads 12. Then, the space between the semiconductor chip 16 and the multilayer wiring film 15 is filled by underfill 17, and the underfill 17 is cured. The BGA solder balls 19 are mounted onto the pads on the surface of
15 the printed circuit board 24. Similarly to the first through third embodiments, the semiconductor chip 16 may be mounted on the multilayer wiring film 15 by wire bonding or the like.

The semiconductor package board 31d or the semiconductor device of the fifth embodiment structured as described above has the
20 enhanced function of a ground layer because of the provision of a printed circuit board 24 as a carrier base. The semiconductor package board 31c can be readily provided with additional functions by incorporating passive components such as resistors or capacitors within the printed circuit board 24. The printed circuit board 24 also
25 helps alleviate the stress generated in the secondary mounting

operation, thereby improving reliability of the semiconductor device.

Next, a semiconductor package board or a semiconductor device according to a sixth embodiment of the present invention will be described.

Fig. 7 is a partial sectional view showing the structure of the semiconductor device according to the sixth embodiment of the present invention.

As shown in Fig. 7, the characteristic feature of the semiconductor package board 31f of the sixth embodiment is that the semiconductor package boards 31a, 31b or 31c according to the first through fourth embodiments are provided with a printed circuit board 24a as a carrier base. Electrical connection between the semiconductor package boards 31a, 31b or 31c and printed circuit board 24a is achieved by an anisotropic conductive film or conductive paste 23. Additionally, the through-holes 30 in the printed circuit board 24a are fitted with connector pins 25.

Similarly to the above-described fifth embodiment, the carrier base may be bonded to the semiconductor package board by any suitable means such as an adhesive, thermo-compressive bonding, or chemical reaction. The electrical connection is achieved by an anisotropic conductive film or conductive paste 23 in a desired pattern. In the example illustrated in Fig. 7, a printed circuit board 24a is used for the carrier base, and the through-holes 30 of the printed circuit board 24a are fitted with connector pins 25 for achieving electrical connection to the outside. The connector pins 25 do not need to be positioned exactly above the metal pads 29 through which the printed

circuit board 24a is connected to the multilayer wiring film 15.

The semiconductor device according to the sixth embodiment is composed of the semiconductor package board 31f and a semiconductor chip 16 mounted thereon, and is assembled as follows.

5 The printed circuit board 24a is bonded by an adhesive 22 to a semiconductor package board 31a, 31b or 31c of the above-described first through fourth embodiments. In this way, the electrical connection is achieved in the desired positions, thereby obtaining the semiconductor package board 31f as shown in Fig. 7. The
10 semiconductor chip 16 is flip-chip bonded so as to be electrically connected to the metal pads 12 of the semiconductor package board 31f. Then, the space between the semiconductor chip 16 and the multilayer wiring film 15 is filled by underfill 17, and the underfill 17 is cured. The connector pins 25 are mounted onto the through-holes
15 30 of the printed circuit board 24a. Similarly to the first through fourth embodiments, the semiconductor chip 16 may be mounted on the multilayer wiring film 15 by wire bonding or the like.

The semiconductor package board 31g or the semiconductor device of the sixth embodiment structured as described above has the
20 enhanced function of a ground layer, similarly to the fifth embodiment, due to the provision of a printed circuit board 24a as a carrier base. The semiconductor package board 31f can be readily provided with additional functions by incorporating passive components such as resistors or capacitors within the printed circuit board 24a. The
25 printed circuit board 24a also helps alleviate the stress generated in the

secondary mounting operation, thereby improving reliability of the semiconductor device. Furthermore, connector pins 25 can be securely attached to the printed circuit board 24a by using its via-holes.

Next, a semiconductor package board or a semiconductor device according to a seventh embodiment of the present invention will be described. Fig. 7 is a partial sectional view showing the structure of the semiconductor device according to the sixth embodiment of the present invention.

As shown in Fig. 8, the characteristic feature of the semiconductor package board 31e of the seventh embodiment is that is the semiconductor package board 31a, 31b or 31c according to the first through fourth embodiments are provided with a ceramic board 26 as a carrier base.

The semiconductor device according to the seventh embodiment is composed of the semiconductor package board 31e and a semiconductor chip 16 mounted thereon, and is assembled as follows. The ceramic board 26 is bonded by an adhesive 22 to a semiconductor package board 31a, 31b or 31c of the above described first through fourth embodiments, such that electrical connection is achieved in the desired positions. The semiconductor package board 31e is thereby obtained, as shown in Fig. 8. The semiconductor chip 16 is flip-chip bonded so as to be electrically connected to the metal pads 12 of the semiconductor package board 31d. Then, the space between the semiconductor chip 16 and the multilayer wiring film 15 is filled with underfill 17, and the underfill 17 is cured. The BGA

solder balls 19 are mounted on corresponding pads provided in the ceramic board 26. The BGA solder balls 19 may be located just above the via holes. Similarly to the first through fourth embodiments, the semiconductor chip 16 may be mounted on the
5 multilayer wiring film 15 by wire bonding or the like.

The semiconductor package board 31e or the semiconductor device of the sixth embodiment structured as described above has the enhanced function of a ground layer due to the provision of a ceramic board 26 as a carrier base. The semiconductor package board 31e
10 can be readily provided with additional functions by incorporating passive components such as resistors or capacitors within the ceramic board 26. The ceramic board 26 also helps alleviate the stress generated in the secondary mounting operation, thus improving reliability of the semiconductor device.

15 Next, several examples of the method for fabricating a semiconductor device according to the present invention will be described. Figs. 9A through 9I are partial sectional views illustrating a semiconductor device fabricating method according to a first example of the method of the present invention. The views are in the
20 same order as the process steps. The method of the present embodiment is used for fabricating the semiconductor device according to the first embodiment of the present invention shown in Figs. 1A to 1C. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the
25 next step.

First, a resist plate 27 is formed on the surface of the metal base 11 made of a metal plate having a thickness in a range of 0.1 to 1.5 mm as shown in Fig. 9A. A fluid resist plate 27 may be provided by any technique such as spin coating, die coating, curtain coating, or printing. If the resist plate 27 is made of a dry film, it can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by a drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Next, as shown in Fig. 9B, at least one metal which is selected from the group consisting of gold, tin, and solder, or an alloy thereof is precipitated in the openings in the resist plate 27. This is achieved by electrolytic plating or electroless plating so as to form the surface layers of the first metal pads 12. Nickel as a barrier metal (not shown) and copper are consecutively precipitated to complete the first metal pads 12. A barrier metal such as nickel may also be precipitated in the openings in the resist plate 27 prior to the formation of the surface layers of the metal pads 12. This is achieved in order to prevent an intermetallic compound from being formed between the metal base 11 and the surface layers of the metal pads 12. Such a barrier metal should preferably be made of a metal which allows itself to be readily removed by etching. If the surface of the metal pads 12 is desired to be retracted from the surface of the multilayer wiring film

15 in successive process steps shown in Figs. 9A to 9D, metal such as nickel which is removable by etching is first precipitated to a predetermined thickness. This is followed by the precipitation of metals constituting the surface layers of the metal pads 12, nickel as a
5 barrier metal, and copper to complete the metal pads 12.

Then, the resist plate 27 is removed as shown in Fig. 9C, and the surface of the metal base 11 with the metal pads 12 is thoroughly cleaned.

Next, the insulating layer 13 is formed as shown in Fig. 9D.
10 Fluid insulating resin may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. After that, the insulating resin is cured by drying treatment or the like. Predetermined patterns
15 including the through holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not. Finally, the insulating resin is cured to complete the insulating layer 13.

Next, the wiring layer 14 including a pattern of electrically
20 conductive material is formed by any of the subtractive, semi-additive, or full-additive techniques. The through holes 34 are filled with a conductive material for connecting the wiring layer 14 to the metal pads 12.

The process steps for forming the insulating layer 13 and the
25 wiring layer 14 using any of the subtractive, semi-additive, or full-

additive techniques are repeated for forming the multilayer wiring film 15 as shown in Fig. 9F.

Next, an etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and on the front surface of the metal base 11 as shown in Fig. 9G. The etching resist may be deposited by any method such as spin coating, die coating, curtain coating, or printing if it is fluid, or by a laminating method if it is made of a dry film.

Thereafter, the etching resist 28 is cured by a drying treatment or the like, and a predetermined pattern is formed therein either by a photolithographic process or a laser processing method depending on whether the etching resist 28 is photosensitive or not. The metal base 11 is then etched, using the etching resist 28 as a mask, until the multilayer wiring film 15 is exposed so as to form a recess 32.

The etching resist 28 is then removed as shown in Fig. 9H, and the surface of the metal pads 12 and the surface of the metal pads 29 are thoroughly cleaned. Thus the semiconductor package board 31a is obtained.

Next, the semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18 as shown in Fig. 9I, after which the space between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, and the underfill 17 is cured.

Finally, the BGA solder balls 19 are mounted onto the metal pads 29, thereby completing the semiconductor device as shown in Fig. 9D.

Thus the semiconductor devices according to the first embodiment of the present invention previously described are efficiently manufactured by the above described fabrication process. According to the first example of the method of the present invention,
5 the multilayer wiring film 15 is laminated on the planar metal base 11 which serves as a support, whereby the smoothness of the multilayer wiring film 15, particularly of its front surface, on which the semiconductor chip 16 is connected, is improved.

Next, a semiconductor device fabrication process according to a
10 second example of the method of the present invention will be described. The method according to the second example is used for manufacturing the semiconductor device according to the second embodiment of the present invention previously described, and shown in Fig. 2. The characteristic feature of the present example is,
15 compared to the method according to the first example, that it has an additional process step for forming a metallic film 35. Figs. 10A through 10K are partial sectional views illustrating a semiconductor device fabrication process according to the second example of the method of the present invention. The views are arranged in the same
20 order as the process steps. Although not illustrated, cleaning and thermal processing are performed as required after a process step prior to the next step.

First, a resist plate 27 is formed on the surface of the metal base 11 composed of a metal plate having a thickness in a range of 0.1 to
25 1.5 mm as shown in Fig. 10A. The resist plate 27 may be formed by

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any technique such as spin coating, die coating, curtain coating, or printing, if it is fluid. Alternatively, resist plate 27 made of a dry film can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Next, as shown in Fig. 10B, a metal selected from the group consisting of gold, tin and solder or an alloy thereof is precipitated in the openings in the resist plate 27 by electrolytic plating or electroless plating to form a surface layers of the first metal pads 12, after which nickel as barrier metal (not shown) and copper are consecutively precipitated to form the first metal pads 12. A barrier metal such as nickel may also be precipitated in the openings in the resist plate 27 prior to the formation of the surface layers of the metal pads 12. This is conducted in order to prevent an intermetallic compound from being formed between the metal base 11 and the solder balls 20. Such a barrier metal should preferably be made of a metal which allows itself to be readily removed by etching.

In addition, if the surface of the metal pads 12 should be retracted from the surface of the multilayer wiring film 15, the metal constituting the metal pads 12 is precipitated after precipitation of nickel, for example, which is readily removed by etching, to a specified thickness, then nickel is precipitated as a barrier metal, and

copper is finally precipitated to form a final structure of the metal pads 12.

Thereafter, as shown in Fig. 10C, a resist plate 36 is formed. In this step, it is generally preferable that the resist plate 36 is formed after the resist plate 27 is removed. Alternatively, the resist plate 36 may be formed on the resist plate 27, followed by patterning of the resist plate 36 together with the resist plate 27. The resist plate 36 may be formed by any technique such as spin coating, die coating, curtain coating, or printing, if it is fluid. Alternatively, a resist plate 36 made of a dry film can be formed by a laminating method or the like.

Thereafter, the resist plate 36 is cured by drying treatment or the like. A predetermined pattern is then formed in the resist plate 36 by a photolithographic process or the like. If the resist plate 36 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Next, as shown in Fig. 10D, at least one metal which is selected from the group consisting of gold, platinum, silver, palladium, titanium, chrome, molybdenum, tantalum, nickel and aluminum, or an alloy thereof, which have a large resistance against the etching for the metal base 11, is precipitated in the openings in the resist plate 36.

This is achieved by electrolytic plating or electroless plating so as to form a surface layer for a metallic film 35. Next, the metallic film 35 is formed by precipitating copper, nickel or palladium using electrolytic plating or electroless plating, for obtaining a desired thickness of the metallic film 35. If it is desired that the metallic film

have an additional electric property, a barrier metal not shown may be formed for suppressing intermetallic diffusion. In this case, if it is considered that an intermetallic compound is formed between the metal in the metal base 11 and the metal constituting the surface layer of the metallic film 35, a nickel barrier metal is formed prior to the formation of the surface layer of the metal pads 12. This barrier metal is preferably made of a metal that is readily removed by etching. In addition, if the surface of the metallic film 35 is to be retraced from the surface of the multilayer wiring film 15 in the later steps, the metallic film 35 should be formed after precipitation of a metal, such as nickel which is readily removed by etching, to a desired thickness. Conversely, if the metallic film 35 should protrude from the multilayer wiring film 15, a recess is formed by etching using a resist plate 36 as a mask before forming the metallic film 35.

Then, the resist plate 27 is removed as shown in Fig. 10E, and the surface of the metal base 11 is thoroughly cleaned.

Next, an insulating layer 13 is formed as shown in Fig. 10F. Fluid insulating resin for the insulating layer 13 may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. Thereafter, the insulating resin is cured by a drying treatment or the like.

Predetermined patterns including the via holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not.

Finally, the insulating resin is cured to complete the insulating layer 13.

Next, the wiring layer 14 including a pattern of electrically conductive material is formed by any of the subtractive, semi-additive, or full-additive techniques as shown in Fig. 10G. Via holes 34 are filled with a conductive material for connecting the wiring layer 14 to the metal pads 12. If the metallic film 35 is to be used as an electric component in the electric circuit, via holes are formed at desired positions at the step of Fig. 10F, followed by connecting the wiring layer 14 and the metallic film 35 together in the step of Fig. 10G.

Next, the process steps for forming the insulating layer 13 and the wiring layer 14 using any of the subtractive, semi-additive, or full-additive techniques are repeated for forming the multilayer wiring film 15, as shown in Fig. 10H.

Next, an etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and on the front surface of the metal base 11 as shown in Fig. 10I. The etching resist 28 may be deposited by any of the spin coating, die coating, curtain coating, or printing methods if it is fluid, or by a laminating method if it is made of a dry film.

Thereafter, the etching resist 28 is cured by a drying treatment or the like, and a predetermined pattern is formed therein either by a photolithographic process or a laser processing method depending on whether the etching resist 28 is photosensitive or not. The metal base 11 is then etched, using the etching resist 28 as a mask, until the multilayer wiring film 15 is exposed so as to form a recess 32.

The etching resist 28 is then removed as shown in Fig. 10J, and the surface of the metal pads 12 and the surface of the metal pads 29 are thoroughly cleaned. Thus, the semiconductor package board 31b is obtained.

5 Next, as shown in Fig. 10K, the semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 20, followed by filling the space between the multilayer wiring film 15 and the semiconductor chip 16 with underfill 17 and curing thereof.

10 Finally, the BGA solder balls 19 are mounted on the metal pads 29, thereby completing the semiconductor device as shown in Fig. 10K.

15 In an alternative for the present example, after iterating the steps of Figs. 11A through 11E, the process may advance to the steps beginning with the step of Fig. 10H to form the metallic pads and the metallic film 35 concurrently.

20 As shown in Fig. 11A, a resist plate 27 is formed on the surface of the metal base 11 composed of a metal plate having a thickness in a range of 0.1 to 1.5 mm. The resist plate 27 may be formed by any technique such as spin coating, die coating, curtain coating, or printing, if it is fluid. Alternatively, resist plate 27 made of a dry film can be formed on the metal base 11 by a laminating method or the like.

Thereafter, the resist plate 27 is cured by drying treatment or the like.

A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not

25 photosensitive, such a pattern may be formed by a laser processing

method or the like.

Next, as shown in Fig. 11B, a metal selected from the group consisting of gold, tin and solder or an alloy thereof is precipitated in the openings in the resist plate 27 by electrolytic plating or electroless plating to form surface layers of the metallic film 35 and the metal pads 12, after which nickel as barrier metal (not shown) and copper are consecutively precipitated to form the metallic film 35 and the metal pads 12. A barrier metal such as nickel may be precipitated prior to the formation of the metal pads 12 and the metallic film 35. This is conducted in order to prevent an intermetallic compound from being formed between the metal in the metal base 11 and the surface layers of the metal pads and the metallic film 35. Such a barrier metal should preferably be made of a metal which allows itself to be readily removed by etching.

In addition, if the surfaces of the metal pads 12 and the metallic film 35 should be retracted from the surface of the multilayer wiring film 15, the metal constituting the surfaces of the metal pads 12 and the metallic film 35 is precipitated after precipitation of nickel, for example, which is readily removed by etching, to a specified thickness, then nickel is precipitated as a barrier metal, and copper is finally precipitated to form the final structure of the metal pads 12 and the metallic film 35.

Thereafter, as shown in Fig. 11C, the resist plate 27 is removed, and the surface is thoroughly cleaned.

Next, an insulating layer 13 is formed as shown in Fig. 11D.

Fluid insulating resin for the insulating layer 13 may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. Thereafter, the insulating resin is cured by a drying treatment or the like.

Next, the wiring layer 14 including a pattern of electrically conductive material is formed by any of the subtractive, semi-additive, or full-additive techniques as shown in Fig. 11E. Via holes 34 are filled with a conductive material for connecting the wiring layer 14 to the metal pads 12. If the metallic film 35 is to be used as an electric component in the electric circuit, via holes 34 are formed at desired positions at the step of Fig. 11D, followed by connecting the wiring layer 14 and the metallic film 35 together in the step of Fig. 10E.

Thus, the semiconductor device having the metallic film 35 according to the second embodiment previously described is efficiently manufactured by the above described fabrication process. According to the semiconductor device of the present embodiment, the metallic film 35 disposed for the central opening of the metal base 11 alleviates the stress applied to the multilayer wiring film 15, the stress being generated depending on presence or absence of the metal base 11. Thus, generation of cracks can be suppressed in the multilayer wiring film 15.

Next, a semiconductor device fabrication process according to a third example of the method of the present invention will be described. The method according to the third embodiment is used for

manufacturing the semiconductor device according to the third embodiment of the present invention previously described, and shown in Fig. 3. The characteristic feature of the present embodiment is, compared to the method according to the first embodiment, that it has an additional process step for forming solder balls 20 on the surface of the metal pads 12 so as to protrude from the surface of the multilayer wiring film 15. Figs. 12A to 12J are partial sectional views illustrating a semiconductor device fabrication process according to the third example of the method of the present invention. The views are arranged in the same order as the process steps. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step.

First, a resist plate 27 is formed on the surface of the metal base 11 composed of a metal plate having a thickness in a range of 0.1 to 1.5 mm as shown in Fig. 12A. A resist plate 27 may be formed by any technique such as spin coating, die coating, curtain coating, or printing, if it is fluid. Alternatively, resist plate 27 made of a dry film can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Next, as shown in Fig. 12B, half-etching is performed on the metal base 11 using the resist plate 27 as a mask, so as to form

recesses 33 for the solder balls 20 and the metal pads 12 .

Next, as shown in Fig. 12C, the solder balls 20 are formed in the openings in the resist plate 27 by electrolytic plating or electroless plating, after which nickel as barrier metal (not shown) and copper are consecutively precipitated to form the metal pads 12. A barrier metal such as nickel may also be precipitated in the openings in the resist plate 27 prior to the formation of the surface layers of the solder balls 20. This is conducted in order to prevent an intermetallic compound from being formed between the metal base 11 and the solder balls 20. Such a barrier metal should preferably be made of a metal which allows itself to be readily removed by etching.

Thereafter, the resist plate 27 is removed as shown in Fig. 12D, and the surfaces of the metal base 11 and the metal pads 12 is thoroughly cleaned.

Next, the insulating layer 13 is formed as shown in Fig. 12E. Fluid insulating resin for the insulating layer 13 may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. Thereafter, the insulating resin is cured by a drying treatment or the like. Predetermined patterns including the via holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not. Finally, the insulating resin is cured to complete the insulating layer 13. The temperature for setting the insulating layer should be lower

than the melting point of the solder balls 20.

Next, the wiring layer 14 including a pattern of electrically conductive material is formed by any of the subtractive, semi-additive, or full-additive techniques as shown in Fig. 12F. Via holes 34 are
5 filled with a conductive material for connecting the wiring layer 14 to the metal pads 12.

The process steps for forming the insulating layer 13 and the wiring layer 14 using any of the subtractive, semi-additive, or full-additive techniques are repeated for forming the multilayer wiring
10 film 15, as shown in Fig. 12G.

Next, an etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and on the front surface of the metal base 11 as shown in Fig. 12H. The etching resist 28 may be deposited by any of the spin coating, die coating, curtain coating, or printing methods if
15 it is fluid, or by a laminating method if it is made of a dry film.

Thereafter, the etching resist 28 is cured by a drying treatment or the like, and a predetermined pattern is formed therein either by a photolithographic process or a laser processing method depending on whether the etching resist 28 is photosensitive or not. The metal
20 base 11 is then etched, using the etching resist 28 as a mask, until the multilayer wiring film 15 is exposed so as to form a recess 32.

The etching resist 28 is then removed as shown in Fig. 12I, and the surface of the metal pads 12 and the surface of the metal pads 29 are thoroughly cleaned. Thus the semiconductor package board 31b
25 is obtained.

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Next, the semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 20 as shown in Fig. 12J.

Alternatively, this can be conducted through solder balls 18, using the solder balls 20 as supplemental solder. After the space between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, the underfill 17 is cured.

Finally, the BGA solder balls 19 are mounted on the metal pads 29, thereby completing the semiconductor device as shown in Fig. 12J.

The semiconductor devices having the solder balls 20 on the metal pads 12 according to the third embodiment of the present invention are efficiently manufactured by the above described fabrication process. According to the semiconductor device of the present embodiment, the solder balls 20 can function as the main or supplemental solder to flip-chip bond the semiconductor chip 16 to the multilayer wiring film 15, thereby enabling the flip chip pads to be formed at a fine-pitch. Also, the solder balls 18 of the semiconductor chip 16 can be dispensed with.

Next, a semiconductor device fabrication process according to a fourth example of the method of the present invention will be described. Figs. 13A to 13J are partial sectional views illustrating a semiconductor device fabrication process according to the third example of the method of the present invention. The views are arranged in the same order as the process steps. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step. The method according to

the fourth example is used for manufacturing the semiconductor device according to the first embodiment or the second embodiment of the present invention previously described. The characteristic feature of the present example is, compared to the method according to the first example or second example, that it has the process step for forming, in advance, a recess in the metal base 11 for mounting the semiconductor chip therein.

First, a recess 32 for mounting a semiconductor chip therein is formed in the front surface of the metal base 11 composed of a metal plate having a thickness of 0.1 to 1.5 mm, as shown in Fig. 13A. This is achieved either by etching or a cutting process using a drill or the like. Alternatively, the metal base 11 may be composed of a planar metal plate and a metal plate having an opening at a position wherein a semiconductor chip is to be mounted. The planar metal plate and the metal plate are bonded together.

A resist plate 27 is then formed on the rear surface of the metal base 11 as shown in Fig. 13B. Resist plate 27 may be formed by any technique such as spin coating, die coating, curtain coating, or printing if it is fluid. Alternatively, resist plate 27 made of a dry film can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Next, as shown in Fig. 13C, at least one metal which is selected from the group consisting of gold, tin, and solder, or an alloy thereof is precipitated in the openings in the resist plate 27 by electrolytic plating or electroless plating. This is conducted so as to form the surface layers of the metal pads 12. Nickel as a barrier metal (not shown) and copper are consecutively precipitated to complete the metal pads 12. A barrier metal such as nickel may also be precipitated in the openings in the resist plate 27 prior to the formation of the surface layers of the metal pads 12. This is conducted in order to prevent an intermetallic compound from being formed between the metal base 11 and the surface layers of the metal pads 12. Such a barrier metal should preferably be made of a metal which allows itself to be readily removed by etching. If the surface of the metal pads 12 is desired to be retracted from the surface of the multilayer wiring film 15 in later process steps, metal such as nickel which is removable by etching is first precipitated to a predetermined thickness. This is followed by the precipitation of metals constituting the surface layers of the metal pads 12, nickel as barrier metal, and copper, to complete the metal pads 12.

Thereafter, the resist plate 27 is removed as shown in Fig. 13D, and the surface of the metal base 11 with the metal pads 12 is thoroughly cleaned.

Next, the insulating layer 13 is formed as shown in Fig. 13E. Fluid insulating resin for the insulating layer 13 may be deposited by any of the spin coating, die coating, curtain coating, or printing

Predetermined patterns including the via holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not. Finally, the insulating resin is cured to complete the insulating layer 13.

The process steps for forming the insulating layer 13 and the wiring layer 14 using any of the subtractive, semi-additive, or full-additive techniques are repeated for forming the multilayer wiring film 15 as shown in Fig. 13G.

Next, an etching resist 28 is formed in a predetermined pattern on the rear surface of the multilayer wiring film 15 and on the front surface of the metal base 11 as shown in Fig. 13B. The metal base 11 is then etched, using the etching resist 28 as a mask, until the multilayer wiring film 15 is exposed. If the thickness of the metal base 11 within the recess 32 for mounting the semiconductor chip therein is smaller than a predetermined value, it is possible to perform such etching without forming the etching resist 28.

The etching resist 28 is then removed as shown in Fig. 13I, and the surfaces of the metal pads 12 and the surfaces of the metal pads 29 are thoroughly cleaned. Thus the semiconductor package board 31a is obtained.

5 Next, the semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18 as shown in Fig. 13J. After the space between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, the underfill 17 is cured. Finally, the BGA solder balls 19 are mounted on the metal
10 pads 29, thereby completing the semiconductor device as shown in Fig. 13J.

 The semiconductor device obtained by this method has a structure similar to the structure of the semiconductor device manufactured by the method according to the first or second
15 embodiment previously described. According to the fabrication process of the third example of the method of the present invention, the etching time in the process step for etching the metal base 11 shown in Fig. 13H is reduced by providing the recess for mounting the semiconductor chip in the metal base 11 in advance. Also, in this
20 way the openings in the metal base for mounting semiconductor chips therein can be formed uniformly.

 Next, a semiconductor device fabrication process according to a fifth example of the method of the present invention will be described. The method of this fifth example is a combination of the advantages
25 of the above-described third and the fourth examples. Figs. 14A to

14J are partial sectional views illustrating a semiconductor device fabrication process according to the fifth embodiment of the present invention. The views are arranged in the same order as the process steps. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step.

First, a recess 32 for mounting a semiconductor chip therein is formed in the front surface of the metal base 11 composed of a metal plate having a thickness of 0.1 to 1.5 mm. This is achieved by any method previously described in the fabrication process of the third embodiment. A resist plate 27 is then formed on the rear surface of the metal base 11 as shown in Fig. 14A. Resist plate 27 may be formed by any technique such as spin coating, die coating, curtain coating, or printing if it is fluid. Alternatively, resist plate 27 made of a dry film can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by a drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Next, as shown in Fig. 14B, half-etching is performed on the metal base 11 using the resist plate 27 as a mask. This is conducted so as to form recesses 33 for the solder balls 20 and the metal pads 12. In this fourth embodiment of the fabrication process, the recess 32 is formed in the metal base 11 prior to the formation of the recesses 33, but this order may be reversed. Of course, the recess 32 and the

recesses 33 may be simultaneously formed in one step.

Next, as shown in Fig. 14C, solder balls 20 are formed in the openings in the resist plate 27 by electrolytic or electroless plating.

After this nickel as barrier metal (not shown) and copper are

5 consecutively precipitated to form the metal pads 12. A barrier metal such as nickel may also be precipitated in the openings in the resist plate 27 prior to the formation of the surface layers of the solder balls 20 in order to prevent an intermetallic compound from being formed between the metal base 11 and the solder balls 20. Such a barrier
10 metal should preferably be made of a metal which allows itself to be readily removed by etching.

Thereafter, the resist plate 27 is removed as shown in Fig. 14D, and the surface of the metal base 11 with the metal pads 12 is thoroughly cleaned.

15 Next, the insulating layer 13 is formed as shown in Fig. 14E. Fluid insulating resin for the insulating layer 13 may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. Thereafter,
20 the insulating resin is cured by drying treatment or the like.

Predetermined patterns including the via holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not.

Finally, the insulating resin is cured to complete the insulating layer

25 13. Here, the temperature for setting the insulating layer should be

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lower than the melting point of the solder balls 20.

Next, the wiring layer 14 including a pattern of electrically conductive material is formed as shown in Fig. 14F by any of the subtractive, semi-additive, or full-additive techniques. Via holes 34
5 are filled with a conductive material for connecting the wiring layer 14 to the metal pads 12.

The process steps for forming the insulating layer 13 and the wiring layer 14 using any of the subtractive, semi-additive, or full-additive techniques are repeated for forming the multilayer wiring
10 film 15 as shown in Fig. 14G.

Next, an etching resist 28 is formed in a predetermined pattern on the rear surface of the multilayer wiring film 15 and on the front surface of the metal base 11 as shown in Fig. 14H. The metal base 11 is then etched, using the etching resist 28 as a mask, until the
15 multilayer wiring film 15 is exposed. If the thickness of the metal base 11 within the recess 32 for mounting the semiconductor chip therein is smaller than a predetermined value, it is possible to perform such etching without forming the etching resist 28.

The etching resist 28 is then removed as shown in Fig. 14I, and
20 the surface of the metal pads 12 and the surface of the metal pads 29 are thoroughly cleaned. Thus the semiconductor package board 31b is obtained.

Next, the semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 20 as shown in Fig. 14J.

25 Alternatively, this can be achieved through solder balls 18, using the

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solder balls 20 as supplemental solder. After this a gap between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, and the underfill 17 is cured.

Finally, the BGA solder balls 19 are mounted on the metal pads 29, thereby completing the semiconductor device as shown in Fig. 15D.

The semiconductor device obtained by this method has a structure similar to the structure of the semiconductor device manufactured by the method according to the third embodiment previously described. According to the fabrication process of the fifth example of the method of the present invention, the etching time in the process step for etching the metal base 11 is reduced by providing the recess 32 for mounting the semiconductor chip in the metal base 11 in advance. Also, in this way, the openings in the metal base for mounting semiconductor chips therein can be formed uniformly. Moreover, the solder balls 20 formed on the metal pads 12 can function as the main or supplemental solder for flip-chip bonding the semiconductor chip 16 to the multilayer wiring film 15, enabling the flip chip pads to be formed at a fine-pitch. Furthermore, solder balls 18 of the semiconductor chip 16 can be dispensed with.

Next, a semiconductor device fabrication process according to a sixth example of the method of the present invention will be described. The method of this sixth embodiment is used for manufacturing the semiconductor device according to the fourth embodiment of the present invention described above, in which thin-film capacitors 21

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are formed between the metal pads 12 and the wiring layer 14. Figs. 15A and 15B are partial sectional views illustrating a semiconductor device fabrication process according to the sixth example of the method of the present invention. The views are arranged in the same order as the process steps. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step.

First, a metal base 11 formed with metal pads 12 on the surface thereof is obtained by the process steps illustrated in Figs. 9A through 9C. More specifically, a resist plate 27 is formed on the surface of the metal base 11 composed of a metal plate having a thickness in a range of 0.1 to 1.5 mm as shown in Fig. 9A.

Next, as shown in Fig. 9B, at least one metal which is selected from the group consisting of gold, tin, and solder, or an alloy thereof is precipitated in the openings in the resist plate 27 by electrolytic plating or electroless plating to form the surface layers of the metal pads 12. Nickel as a barrier metal and copper are consecutively precipitated to complete the metal pads 12.

Thereafter, the resist plate 27 is removed as shown in Fig. 9C, and the surface of the metal base 11 with the metal pads 12 is cleaned to obtain the structure shown in Fig. 16A.

Instead of obtaining such a metal base 11 with the metal pads 12 formed thereon by the process steps illustrated in Figs. 9A through 9C, a metal base 11 having the metal pads 12 and the solder balls 20 may be prepared by the process steps shown in Figs. 10A through 10E

or Figs 11A through 11C, or else, a metal base having the metal pads 12 and the solder balls 20 may be prepared by the process steps shown in Figs 12A through 12D. Alternatively, the metal base 11 may have a recess 32 for mounting a semiconductor chip therein on its front surface in addition to the metal pads 12 on its rear surface, by the process steps shown in Figs. 13A through 13D. Another possibility is that the metal base 11 may have the recess 32 as well as both of the metal pads 12 and the solder balls 20, by the process steps illustrated in Figs. 14A through 14D. It should be noted that in the case where the metal base 11 has the solder balls 20 therewith, the temperature at which the thin-film capacitors 21 are formed, to be described later, must be lower than the melting point of the solder balls 20.

The metal base 11 having at least the metal pads 12 thereon, as shown in Fig. 15A, is then subjected to film deposition processing such as sputtering, evaporation, CVD, and anodic oxidation, using a suitable resist pattern (not shown) as a mask such that only the surfaces of the desired metal pads 12 are exposed. Thus the thin-film capacitors 21 are formed as shown in Fig. 15B. The dielectric layer of these thin-film capacitors 21 is preferably composed of a compound material having a perovskite structure such as titanium oxide, tantalum oxide, Al_2O_3 , SiO_2 , Nb_2O_5 , BST ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$), PZT ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$), PLZT ($\text{Pb}_{1-y}\text{La}_y\text{Zr}_x\text{Ti}_{1-x}\text{O}_3$), and $\text{SrBi}_2\text{Ta}_2\text{O}_9$, where $0 \leq x \leq 1$ and $0 < y < 1$. Alternatively, the thin-film capacitors 21 may be composed of organic resin or the like with which a desired dielectric constant can be achieved.

Thereafter, unnecessary parts of the dielectric layer are removed by a lift off method wherein the resist is removed at the same time. In this step, the thin-film capacitors 21 can also be placed in desired positions by using a metal mask or the like.

5 The process steps illustrated in Fig. 9D through 9I are then performed sequentially. More specifically, an insulating layer 13 is formed as shown in Fig. 9D, on which a wiring layer 14 having a wiring pattern is formed as shown in Fig. 9E.

10 These processes for forming the insulating layer and the wiring layer are alternately iterated to form the multilayer wiring film 15 as shown in Fig. 9F.

Etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and the front surface of the metal base 11 as shown in Fig. 9G, after which the metal base 11 is etched, using the etching resist 28 as a mask, until part of the multilayer wiring film 15 is exposed.

15 Then, as shown in Fig. 9H, the etching resist 28 is removed, and the surface of the metal pads 12 as well as that of the metal pads 29 are cleaned. Thus the semiconductor package board 31a is completed.

20 Finally, as shown in Fig. 9I, a semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18, and the space between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, and the underfill 17 is cured. The BGA solder balls 19 are then mounted on the metal pads 29. Thus, a

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semiconductor device shown in Fig. 4 having thin-film capacitors 21 between the metal pads 12 and the insulating layer 13 is obtained.

In stead of the metal base 11 having metal pads 12 thereon and obtained by the process steps of Figs. 9A to 9C, the metal base 11 may be used which has the metal pads and the metallic film 35 and is obtained by the process steps of Figs. 10A through 10E or Figs. 11A through 11C. In this case, after the thin-film capacitors 21 is formed, a semiconductor device having the metallic film 35 can be obtained by using the process steps of Fig. 10F through 10K or the process steps of Figs. Figs. 11D, 11E and Figs. 10H through 10K.

In addition, the metal base 11 may be also used which has the metal pads 12 thereon and the recess 32 for mounting therein the semiconductor chip and is obtained by the process steps of Figs. 13A to 13D. In this case, after the thin-film capacitors 21 is formed, the semiconductor device shown in Fig. 4 can be obtained by the process steps of Figs. 13E through 13J. Moreover, the metal base 11 may be also used which has the metal pads 12 and the solder balls 20 as well as the recess 32 for mounting therein the semiconductor chip and is obtained by the process steps of Figs. 14A to 14D. In this case, after the thin-film capacitors 21 is formed, the semiconductor device shown in Fig. 5 can be obtained by the process steps of Figs. 14E to 14J.

Thus, a semiconductor device having a decoupling capacitor in close proximity to the semiconductor chip 16, wherein a thin-film capacitors 21 is formed between at least one metal pad 12 and the wiring layer 14, is manufactured by the fabrication process of the

present example.

Next, a semiconductor device fabrication process according to a seventh example of the method of the present invention will be described. The method of this seventh example is used for manufacturing the semiconductor device according to the fifth embodiment of the present invention described above in which a printed circuit board 24 is bonded thereto as a carrier base. Figs. 16A to 16G are partial sectional views illustrating a semiconductor device fabrication process according to the sixth embodiment of the present invention. The views are arranged in the same order as the process steps. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step.

First, a stacked structure of interconnecting layers (hereafter referred to simply as a "stacked structure") as shown in Fig. 9F, in which the multilayer wiring film 15 is formed on the metal base 11 by the process steps shown in Figs. 9A through 9F, is prepared.

Instead of a stacked structure having the multilayer wiring film 15 on the metal base 11 as shown in Fig. 9F, a stacked structure obtained by the method of the second embodiment shown in Fig. 10H or by the method of the third example shown in Fig. 12G, wherein solder balls 20 are provided, may be used. Alternatively, any of the stacked structures obtained by the methods of the fourth, fifth or sixth examples of the present invention may be used. That is, the stacked structure may include a recess 32 for mounting a semiconductor chip

therein as shown in Fig. 13G, or it may include such a recess 32 and the solder balls 20 as shown in Fig. 14G, or it may include thin-film capacitors 21.

The surface of the multilayer wiring film 15 is cleaned in the step shown in Fig. 13G, and adhesive 22 is applied onto the rear surface of the multilayer wiring film 15 in the regions other than the metal pads 29 as shown in Fig. 13H. The adhesive 22 can be applied in the desired regions by a printing method in which, for example, the metal pads 29 or any other regions on which no adhesive should be applied are masked when applying the adhesive 22, after which the mask is removed. Alternatively, if the adhesive 22 is made of a material having photosensitivity, it may be applied in a desired pattern by a photolithographic process.

Next, a printed circuit board 24 as a carrier base is bonded to the rear surface of the multilayer wiring film 15 such that the metal pads 29 of the film 15 are aligned with the through-holes 30 in the printed circuit board 24 as shown in Fig. 13I. It should be noted that the adhesive 22 may be applied on the printed circuit board 24 instead of on the rear surface of the multilayer wiring film 15 as in the example shown in Fig. 13H.

The through-holes 30 in the printed circuit board 24 are then filled with conductive paste 23 as shown in Fig. 17D, and cured by applying heat. If there is the risk that the conductive paste 23 may leak or deform in successive process steps, it is preferable that the through-holes 30 be additionally filled with insulating resin, and the

insulating resin be cured.

Next, an etching resist 28 is formed on the surfaces of the printed circuit board 24, inner walls of the through-holes 30, and the metal base 11 as shown in Fig. 14A. The etching resist 28 may be formed by any technique such as spin coating, die coating, curtain coating, or printing if it is fluid, or by a laminating method if it is a dry film. Thereafter, the etching resist 28 is cured by a drying treatment or the like. A predetermined pattern is then formed in the etching resist by a photolithographic process or the like. If the etching resist 28 is not photosensitive, such a pattern may be formed by a laser processing method or the like. Thereafter, the metal base 11 is etched using this etching resist 28 as a mask until part of the multilayer wiring film 15 is exposed. In the case where the metal base 11 has a recess 32 for mounting the semiconductor chip therein, if the thickness of the metal base 11 within the recess 32 is smaller than a predetermined value, it is possible to perform such etching without forming the etching resist 28.

The etching resist 28 is then removed as shown in Fig. 14B, and the surface of the metal pads 12 and the surface of the metal pads on the printed circuit board 24 are thoroughly cleaned. Thus, the semiconductor package board 31d is obtained.

Next, a semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18 as shown in Fig. 14C. If the solder balls 20 are provided on the surfaces of the metal pads 12, the semiconductor chip is flip-chip bonded via the solder balls 20 or via

solder balls 18 by using the solder balls 20 as supplementary solder. After the space between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, the underfill 17 is cured. Finally, the BGA solder balls 19 are mounted on the metal
5 pads of the printed circuit board 24.

As a modification of the above-described seventh example, the printed circuit board 24a described in the sixth embodiment of the semiconductor device of the present invention may be used. That is, the through-holes 30 may be fitted with connector pins 25 instead of
10 mounting the BGA solder balls 19 on the metal pads, after the semiconductor chip 16 is flip-chip mounted on the metal pads 12.

Thus, the semiconductor device provided with a carrier base as shown in Fig. 6C or Fig. 7 can be efficiently manufactured according to the method of the present example.

15 Next, a semiconductor device fabrication process according to a eighth embodiment of the present invention will be described. Figs. 17A to 17C are partial sectional views illustrating a semiconductor device fabrication process according to the seventh embodiment of the present invention. The views are arranged in the same order as the
20 process steps. The method of this seventh embodiment is used for manufacturing the semiconductor devices having a carrier base bonded thereto. Compared to the method of the sixth embodiment described above, the method of the seventh embodiment is characterized in that it uses a carrier base having via-holes filled with
25 conductive material, or a carrier base provided with additional

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connection pads. The carrier base may be either a printed circuit board, a ceramic board, or an organic/inorganic composite board. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step.

5 Similarly to the method of the seventh embodiment, a stacked structure of interconnecting layers in which the multilayer wiring film 15 is formed on the metal base 11 is first fabricated by the process steps shown in Figs. 9A through 9F. A stacked structure as shown in Fig. 10H and having the metallic film 35 or a stacked structure as
10 shown in Fig. 12G and having the solder balls 20, obtained by the method of the second or third example, may be used instead of the stacked structure shown in Fig. 9F. Alternatively, a stacked structure having a recess 32 for mounting a semiconductor chip therein as shown in Fig. 13G, obtained by the method of the fourth example,
15 may be used. Another possibility is that the stacked structure may include the recess 32 as well as the solder balls 20 as shown in Fig. 14G, and described in the method of the fifth example, or it may include thin-film capacitors 21 as described in the method of the sixth example.

20 The surface of the multilayer wiring film 15 is cleaned in the step shown in Fig. 17A, and adhesive 22 is applied on the rear surface of the multilayer wiring film 15 in the regions other than the metal pads 29 as shown in Fig. 17B. The adhesive 22 is applied in the desired regions by any of the methods mentioned in the above-
25 described sixth embodiment.

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Next, a ceramic board 26 as a carrier base is bonded to the multilayer wiring film 15 such that the pads on the ceramic board 26 are connected to the pattern of conductive paste 23 as shown in Fig. 17C. In the present embodiment, as illustrated in Fig. 17C, in order to bond the ceramic board 26 to the multilayer wiring film 15, the front surface of the multilayer wiring film 15 is coated with the adhesive 22 and conductive paste 23. Both of these may of course be applied on the front surface of the ceramic board 26, or they may individually be provided on either one of the front surface of the multilayer wiring film 15 and the front surface of the ceramic board 26.

The process steps which are similar to those shown in Figs. 16E to 16G are successively performed. That is, an etching resist 28 is formed on the surfaces of the ceramic board 26 and the metal base 11 in a predetermined pattern, after which the metal base 11 is etched using this etching resist 28 as a mask until part of the multilayer wiring film 15 is exposed. The etching resist 28 is then removed, and the surface of the metal pads 12 and the surface of the metal pads on the ceramic board 26 are thoroughly cleaned. Thus a semiconductor package board is obtained.

Next, a semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18, after which a gap between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, and the underfill 17 is cured. Finally, the BGA solder balls 19 are mounted onto the metal pads of the ceramic board 26.

As one modification of the above-described eighth example, connector pins 25 may be mounted instead of the BGA solder balls 19, after the semiconductor chip 16 is flip-chip bonded to the metal pads 12.

Thus, according to the method of the seventh example, a semiconductor package board provided with a carrier base in which via-holes are filled with conductive material as shown in Fig. 7 or a carrier base having additional connection pads can be efficiently manufactured.

Next, a semiconductor device fabrication process according to a ninth example of the method of the present invention will be described. Figs. 18A through 18E are partial sectional views illustrating a semiconductor device fabrication process according to the ninth example of the method of the present invention. The views are arranged in the same order as the process steps. The method of this ninth example is used for manufacturing the semiconductor device according to the fifth embodiment of the present invention described above, having a carrier base bonded thereto. The method of the present example is characterized in that an opening is first formed in the metal base 11 for receiving a semiconductor chip 16 therein before bonding the metal base 11 to the carrier base. Although not illustrated, cleaning and thermal processing are performed as required after the process step prior to the next step.

In the example illustrated in Figs. 18A through 18E, a printed circuit board 24 is used for the carrier base similarly to the method of

the seventh example. These drawings exemplarily show the process steps which are performed on the metal base 11 shown in Fig. 9H on which the multilayer wiring film 15 is stacked and in which an opening is formed. Instead of such a metal base, any of those shown in Fig. 10J, Fig. 12I, Fig. 13I or Fig. 14I, or the one having thin-film capacitors 21 obtained by the method of the sixth embodiment, may be used.

First, the metal base 11 having the multilayer wiring film 15 thereon and an opening therein is obtained by the process steps illustrated in Figs. 9A through 9G. More specifically, a resist plate 27 is formed on the surface of the metal base 11 composed of a metal plate having a thickness in a range of 0.1 to 1.5 mm in a predetermined pattern, as shown in Fig. 9A.

Next, as shown in Fig. 9B, at least one metal which is selected from the group consisting of gold, tin, and solder, or an alloy thereof is precipitated in the openings in the resist plate 27 by electrolytic plating or electroless plating. This is followed by precipitation of nickel as a barrier metal and of copper, so as to form the metal pads 12.

Thereafter, the resist plate 27 is removed as shown in Fig. 9C, the surface of the metal base 11 with the metal pads 12 is cleaned, an insulating layer 13 is formed as shown in Fig. 9D, and a wiring layer 14 including a pattern of interconnections is formed as shown in Fig. 9E.

The processes required to form the insulating layer and the wiring layer are alternately iterated to form the multilayer wiring film

15, thereby obtaining a stacked structure as shown in Fig. 9F. Next, an etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and the front surface of the metal base 11 as shown in Fig. 9G in a predetermined pattern, after which the metal base 11 is
5 etched, using the etching resist 28 as a mask, until part of the multilayer wiring film 15 is exposed.

The surface of the multilayer wiring film 15 is cleaned in the step shown in Fig. 18A, and adhesive 22 is applied on the rear surface of the multilayer wiring film 15 in the regions other than the metal
10 pads 29 as shown in Fig. 18B.

Next, a printed circuit board 24 as a carrier base is bonded to the multilayer wiring film 15 such that the metal pads 29 of the multilayer wiring film 15 are aligned with the through-holes 30 in the printed circuit board 24 as shown in Fig. 18C. In the present
15 embodiment, as illustrated in Fig. 18B, the front surface of the multilayer wiring film 15 is coated with the adhesive 22. However, the adhesive 22 may be applied onto the printed circuit board 24 for the purpose of bonding.

The through-holes 30 in the printed circuit board 24 are then
20 filled with conductive paste 23 as shown in Fig. 18D, and the conductive paste 23 is cured by applying heat. If there is the risk that the conductive paste 23 may leak or deform in the succeeding process steps, it is preferable that the through-holes 30 be additionally filled with insulating resin, and the insulating resin be cured. Thus the
25 semiconductor package board 31c as shown in Fig. 18D is obtained.

Next, a semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18 as shown in Fig. 21B. If solder balls 20 are formed on the surface of the metal pads 12, the semiconductor chip 16 is flip-chip bonded via the solder balls 20, or via the solder balls 18 by using the solder balls 20 as a supplementary solder. Thereafter, the space between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, and the underfill 17 is cured. Finally, the BGA solder balls 19 are mounted onto the metal pads of the printed circuit board 24.

As a modification of the above-described method of the ninth example of the method of the present invention, the printed circuit board 24a described in the sixth embodiment of the semiconductor device of the present invention may be used. More specifically, the through-holes 30 may be fitted with the connector pins 25 instead of mounting the BGA solder balls 19 on the metal pads, after the semiconductor chip 16 is flip-chip bonded to the metal pads 12.

According to the fabrication process of the ninth example of the method of the present invention, an opening is formed in the metal base 11 for receiving a semiconductor chip 16 therein, before bonding a carrier base to the metal base 11. Therefore, the etching process of the metal base 11 after the bonding of the carrier base thereto is dispensed with. With respect to the bonding between the multilayer wiring film 15 and the carrier base, it is advantageous to use a method according to either the seventh or the eighth embodiments. On the other hand, the method according to the ninth embodiment is

preferable if the carrier base consists of a material which is susceptible to damage by the etching process.

Next, a semiconductor device fabrication process according to a tenth example of the method of the present invention will be described.

5 Figs. 19A to 19C are partial sectional views illustrating a semiconductor device fabrication process according to the tenth example of the method of the present invention. The views are arranged in the same order as the process steps. This embodiment is a combination of the methods according to the above-described eighth
10 example and the ninth example, and it is used for manufacturing the semiconductor package board having a carrier base bonded thereto. The method of the tenth example is characterized in that it uses a carrier base having via-holes filled with conductive material, or a carrier base provided with additional connection pads. Also, it is
15 characterized in that an opening is first formed in the metal base 11 for receiving a semiconductor chip 16 therein before bonding the carrier base to the multilayer wiring film 15. The carrier base may be either a printed circuit board, a ceramic board, or an organic/inorganic composite board. Although not illustrated, cleaning and thermal
20 processing are performed as required after the process step prior to the next step.

In the example illustrated in Figs. 19A to 19C, a ceramic board is used for the carrier base. These drawings exemplarily show the process steps which are performed on the metal base 11 shown in Fig.
25 9H on which the multilayer wiring film 15 is formed. Instead of

such a metal base, any of those shown in Fig. 10J, Fig. 12I, Fig. 13I or Fig. 14I, or the one having thin-film capacitors 21 obtained by the method of the sixth embodiment, may be used.

First, similarly to the method of the eighth example, the metal
5 base 11 having the multilayer wiring film 15 thereon is obtained by the process steps illustrated in Figs. 9A to 9G.

Fig. 19A shows the state after the etching resist 28 is removed. The surface of the multilayer wiring film 15 is cleaned, and adhesive 22 is applied onto the rear surface of the multilayer wiring film 15 in the regions other than the metal pads 29 as shown in Fig. 19B.
10 Conductive paste 23 is then placed in the positions corresponding to the metal pads 29 located in the openings in the layer of adhesive 22. Alternatively, the conductive paste 23 may first be placed in desired the positions, after which the adhesive may be applied.

15 Next, a ceramic board 26 as a carrier base is bonded to the multilayer wiring film 15 such that the metal pads on the ceramic board 26 are connected to the pattern of conductive paste 23 as shown in Fig. 19C. In the present embodiment, as illustrated in Fig. 19B, in order to bond the ceramic board 26 to the multilayer wiring film 15,
20 the front surface of the multilayer wiring film 15 is coated with the adhesive 22 and the conductive paste 23. Both of these may be applied on the front surface of the ceramic board 26, or they may individually be provided on either one of the front surface of the multilayer wiring film 15 and the front surface of the ceramic board
25 26. Thus a semiconductor package board 31d shown in Fig. 19C is

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obtained.

The process step thereafter is similar to that shown in Fig. 16G. A semiconductor chip 16 is flip-chip bonded to the metal pads 12 through the solder balls 18, after which a gap between the multilayer wiring film 15 and the semiconductor chip 16 is filled with underfill 17, and the underfill 17 is cured. Finally, the BGA solder balls 19 are mounted onto the metal pads of the ceramic board 26.

As a modification of the above-described tenth embodiment, the printed circuit board 24a described in the sixth embodiment of the semiconductor device of the present invention may be used. That is, the through-holes 30 may be fitted with connector pins 25 instead of mounting the BGA solder balls 19 on the metal pads, after the semiconductor chip 16 is flip-chip mounted on the metal pads 12.

Thus, according to the method of the tenth embodiment, semiconductor package boards provided with a carrier base in which via-holes are filled with conductive material or a carrier base having additional connection pads can be efficiently manufactured. Moreover, since a recess is formed in the metal base 11 for receiving a semiconductor chip 16 therein before bonding a carrier base to the multilayer wiring film 15, the etching process of the metal base 11 after the bonding of the carrier base can be omitted. In this way, a carrier base which is susceptible to damage by the etching process can be used.

Next, a method according to an eleventh example of the method of the present invention will be described with reference to Figs. 20A

to 20G which consecutively show the process in sectional views of the semiconductor device. The steps following the step of Fig. 20G are similar to those shown in Figs. 9F through 9I.

In the feature of the present example, both the surfaces of the metal base 11 are provided with the metal pads 12 and the multilayer wiring film 15, followed by separation of the metal base 11 to obtain a pair of package boards each having a second or front surface. This allows the throughput of the fabrication of the semiconductor package boards to double.

The process steps of Figs. 20A to 20F are similar to those in the first example of the method of the present invention. Alternatively, the process steps in the second example shown in Figs. 10A to 10G or Figs. 11A to 11E, the process steps shown in Figs. 10H to 10K, the process steps in the third example shown in Figs. 12A to 12F, the process steps shown in Figs. 12G to 12J, or the process steps in the sixth example using the thin-film capacitors 21 may be used instead. Between the steps, suitable cleaning and thermal processing steps may be used.

First, as shown in Fig. 20A, a resist plate 27 is formed on each of both the surfaces of the original metal base 11 made of metal plate. For obtaining a thickness of 0.1 to 1.5 mm for each of the metal base after the separation of the original metal base 11, the original metal base preferably has a thickness of 0.2 to 3.0 mm. A fluid resist plate 27 may be provided by any technique such as spin coating, die coating, curtain coating, or printing. If the resist plate 27 is made of a dry

film, it can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by a drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Subsequently, as shown in Fig. 20B, at least one metal selected from the group consisting of gold, tin and solder or an alloy thereof is precipitated in the openings in the resist plate 27 by using an electrolytic plating or electroless plating technique, thereby forming the surface layers of the first metal pads 12. Then, nickel as a barrier metal and copper are consecutively precipitated to form first metal pads 12. If it is considered that an intermetallic compound is formed between the metal in the metal pads 12 and the metal in the surface layers of the metal pads 12, nickel is precipitated as the barrier metal before the surface layers of the metal pads 12 are formed. In this case, the barrier metal is preferably made of a metal that can be readily removed by etching. In addition, if it is desired that the surface of the metal pads 12 be retracted from the surface of the multilayer wiring film 15 in the following steps such as shown in Figs. 9F through 9I, a metal such as nickel that can be readily removed by etching is first precipitated to a specified thickness, followed by consecutive precipitation of the metal for the surface layers of the metal pads, nickel as a barrier metal and copper to form the metal pads 12.

Then, the resist plate 27 is removed as shown in Fig. 20C, and the surface of the metal base 11 with the metal pads 12 is thoroughly cleaned.

Next, the insulating layer 13 is formed on each of the surfaces of the original metal base 11, as shown in Fig. 20D. In this step, fluid insulating resin may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. After that, the insulating resin is cured by drying treatment or the like. Predetermined patterns including the through holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not. Finally, the insulating resin is cured to complete the insulating layer 13.

Next, as shown in Fig. 20E, the wiring layer 14 including a pattern of electrically conductive material is formed by any of the subtractive, semi-additive, or full-additive techniques on each of both the surfaces of the original metal base 11. The through holes 34 are filled with a conductive material for connecting the wiring layer 14 to the metal pads 12.

The process steps for forming the insulating layer 13 and the wiring layer 14 using any of the subtractive, semi-additive, or full-additive techniques are repeated for forming the multilayer wiring film 15 on each of both the surfaces of the original metal base 11 as shown in Fig. 20F.

Next, as shown in Fig. 20G, the original metal base 11 is separated by using a slicing die or cutter at the center of the metal base 11 as viewed in the thickness direction thereof, thereby obtaining a pair of package boards.

5 The subsequent steps are similar to the steps shown in Figs. 9G through 9I. More specifically, an etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and the front surface of the separated metal base 11A, followed by etching the metal base 11 by using the etching resist 28 as a mask to form the recess 32 and to
10 expose front surface of the multilayer wiring film 15. Then, the etching resist 28 is removed, the surface of the metal base with the multilayer wiring film 15 is cleaned, to obtain the structure of the semiconductor packaging board 31a of the present embodiment.

Subsequently, as shown in Fig. 9I, the semiconductor chip 16 is
15 flip-chip bonded to the metal pads 12 via the solder balls 18, followed by filling the space between the multilayer wiring film 15 and the semiconductor chip 16 with underfill 17, and curing the same.

Thereafter, BGA solder balls 19 are mounted onto the metal pads 29, to obtain the semiconductor device shown in Fig. 9I.

20 It is to be noted that the semiconductor device bonded to the carrier base can be fabricated using the method according to the seventh example or eighth example. In this case, the carrier base may be bonded to the metal base after separation of the original metal base, or else the original metal base may be separated after the carrier bases
25 are bonded to the multilayer wiring films formed on both the surfaces

of the original metal base.

Next, a method according to a twelfth example of the method of the present invention will be described with reference to Figs. 21A to 21H which consecutively show the process in sectional views of the semiconductor device. The steps following the step of Fig. 21H are similar to those shown in Figs. 9F through 9I.

In the feature of the present example, a pair of metal bases are bonded together to form a bonded metal base, and both the surfaces of the bonded metal base are provided with the metal pads 12 and the multilayer wiring film 15, followed by separation of the bonded metal base 11 to obtain a pair of metal bases 11 each having a flat second surface. This allows the throughput of the fabrication of the semiconductor package boards to double.

The process steps of Figs. 21A to 21F are similar to those in the first example of the method of the present invention. Alternatively, the process steps in the second example shown in Figs. 10A to 10G or Figs. 11A to 11E, the process steps shown in Figs. 10H to 10K, the process steps in the third example shown in Figs. 12A to 12F, the process steps shown in Figs. 12G to 12J, or the process steps in the sixth example using the thin-film capacitors 21 may be used instead. Between the steps, suitable cleaning and thermal processing steps may be used.

First, as shown in Fig. 21A, a pair of metal bases 11 each made of a metal plate having a thickness of 0.1 to 1.5 mm are bonded together to form a bonded metal base. Each metal base may have a

recess 32. The bonding may be conducted after forming ruggedness on the surfaces of the pair of metal bases 11 to be bonded together. Alternatively, the bonding may be achieved by using adhesive or welding at the entire surface or at the periphery thereof. It is
5 preferable to bond the surfaces together at the periphery thereof in view of later separation.

Subsequently, as shown in Fig. 21B a resist plate 27 is formed on each of both the surfaces of the bonded metal base. A fluid resist plate 27 may be provided by any technique such as spin coating, die
10 coating, curtain coating, or printing. If the resist plate 27 is made of a dry film, it can be formed on the metal base 11 by a laminating method or the like. Thereafter, the resist plate 27 is cured by a drying treatment or the like. A predetermined pattern is then formed in the resist plate 27 by a photolithographic process or the like. If the
15 resist plate 27 is not photosensitive, such a pattern may be formed by a laser processing method or the like.

Subsequently, as shown in Fig. 21C, at least one metal selected from the group consisting of gold, tin and solder or an alloy thereof is precipitated in the openings in the resist plate 27 by using an
20 electrolytic plating or electroless plating technique, thereby forming the surface layers of the first metal pads 12. Then, nickel as a barrier metal and copper are consecutively precipitated to form first metal pads 12. If it is considered that an intermetallic compound is formed between the metal in the metal pads 12 and the metal in the surface
25 layers of the metal pads 12, nickel is precipitated as the barrier metal

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before the surface layers of the metal pads 12 are formed. In this case, the barrier metal is preferably made of a metal that can be readily removed by etching. In addition, if it is desired that the surface of the metal pads 12 be retracted from the surface of the multilayer wiring film 15 in the following steps such as shown in Figs. 9F through 9I, a metal such as nickel that can be readily removed by etching is first precipitated to a specified thickness, followed by consecutive precipitation of the metal for the surface layers of the metal pads, nickel as a barrier metal and copper to form the metal pads 12.

Then, the resist plate 27 is removed as shown in Fig. 21D, and the surface of the metal base 11 with the metal pads 12 is thoroughly cleaned.

Next, the insulating layer 13 is formed on each of the surfaces of the bonded metal base, as shown in Fig. 21E. In this step, fluid insulating resin may be deposited by any of the spin coating, die coating, curtain coating, or printing methods. Alternatively, a dry film of insulating resin may be formed on the metal base 11 by a laminating method or the like. After that, the insulating resin is cured by drying treatment or the like. Predetermined patterns including the through holes 34 are then formed either by a photolithographic process or a laser processing method depending on whether the insulating resin is photosensitive or not. Finally, the insulating resin is cured to complete the insulating layer 13.

Next, as shown in Fig. 21F, the wiring layer 14 including a

pattern of electrically conductive material is formed by any of the subtractive, semi-additive, or full-additive techniques on each of both the surfaces of the original metal base 11. The through holes 34 are filled with a conductive material for connecting the wiring layer 14 to the metal pads 12.

The process steps for forming the insulating layer 13 and the wiring layer 14 using any of the subtractive, semi-additive, or full-additive techniques are repeated for forming the multilayer wiring film 15 on each of both the surfaces of the bonded metal base as shown in Fig. 21G.

Next, as shown in Fig. 21H, the bonded metal base is separated by using a slicing die or cutter at the bonded surfaces, thereby obtaining a pair of package boards. If the bonding is conducted only at the periphery of the surfaces, the separation may be achieved by separating the peripheral area of the bonded surface from the central area thereof.

The subsequent steps are similar to the steps shown in Figs. 9G through 9I. More specifically, an etching resist 28 is formed on the rear surface of the multilayer wiring film 15 and the front surface of the separated metal base 11A, followed by etching the metal base 11 by using the etching resist 28 as a mask to form the recess 32 and to expose front surface of the multilayer wiring film 15. Then, the etching resist 28 is removed, the surface of the metal base with the multilayer wiring film 15 is cleaned, to obtain the structure of the semiconductor packaging board 31a of the present embodiment.

Subsequently, as shown in Fig. 9I, the semiconductor chip 16 is flip-chip bonded to the metal pads 12 via the solder balls 18, followed by filling the space between the multilayer wiring film 15 and the semiconductor chip 16 with underfill, and curing the same.

5 Thereafter, BGA solder balls 19 are mounted onto the metal pads 29, to obtain the semiconductor device shown in Fig. 9I.

10 It is to be noted that the semiconductor device bonded to the carrier base can be fabricated using the method according to the seventh example or eighth example. In this case, the carrier base may be bonded to the metal base after separation of the bonded metal base, or else the bonded metal base may be separated after the carrier bases are bonded to the multilayer wiring films formed on both the surfaces of the bonded metal base.

15 As described above, in the semiconductor package board according to the above embodiments, the multilayer wiring film including first metal pads for mounting a semiconductor chip is stacked on a planar metal base, so that it has superior smoothness in the semiconductor chip mounting portion. As a result, the reliability in mounting a semiconductor chip onto a semiconductor package
20 board is improved. The metal base encircling the semiconductor chip also helps prevent warping or dimensional changes of the multilayer wiring film, enabling the multilayer wiring film to have a large number of pins, resulting in its higher density and further miniaturization. The metal base is less deformable compared to a
25 printed circuit board or ceramic board, thus facilitating the realization

of a high density multilayer wiring board.

In the semiconductor device according to the above embodiments, the surface of the semiconductor chip mounted on the package board is disposed substantially coplanar with the surface of the metal base. Therefore, the metal base can be used as a stiffener, whereby a process step for mounting a stiffener to the board is dispensed with and a reduction in production cost is accordingly achieved.

Moreover, solder balls can be placed on the surface of the metal pads for mounting the semiconductor chip. The solder balls allow themselves to be used as solder for mounting the semiconductor chip or supplemental solder, as a result of which the fine-pitch of the pads for the flip-chip bonding can be increased.

Furthermore, according to the present invention, after forming the metal pads on the metal base for mounting a semiconductor chip thereon, thin-film capacitors can further be provided. Therefore, decoupling capacitors can be provided in close proximity to the flip-chip pads of the semiconductor chip.

In addition to the above, the present invention offers various other advantages as follows. In the semiconductor package board to which no carrier base is connected, the conductors are made with a minimum overall length, thereby offering advantages in higher speed signal transmission. With a carrier base, on the other hand, the device's function as a ground layer can readily be enhanced, and various passive components such as resistors and capacitors can also

be added with ease. The carrier base also improves the reliability of the device in a secondary mounting operation, because it helps alleviate the stress generated when mounting the semiconductor package device onto a motherboard.

5 By forming multilayer wiring film on each of both the surfaces of the metal base, the throughput of the semiconductor device can be improved.

10 Since the above embodiments are described only for examples, the present invention is not limited to the above embodiments and various modifications or alterations can be easily made therefrom by those skilled in the art without departing from the scope of the present invention.

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